

Appl. No. 10/711,390
Amdt. dated January 02, 2006
Reply to Office action of December 02, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

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Listing of Claims:

Claim 1 (original): A resistor structure comprising:

- a substrate;
- a semiconductor layer positioned on the substrate;
- 10 a salicide block positioned on portions of the surface of the semiconductor layer; and
at least a salicide layer positioned on the portions of the surface of the semiconductor
layer adjacent to the salicide block;
- wherein the semiconductor layer comprises a predetermined region overlapping the
salicide layer, the junction between the salicide layer and the salicide block, and
- 15 the portions of the salicide block adjacent to the junction between the salicide
layer and the salicide block, and the semiconductor layer has a higher doping
concentration within the predetermined region than in the other regions.

Claim 2: (original) The resistor structure of claim 1 wherein the predetermined region is
20 located at either end of the semiconductor layer.

Claim 3: (original) The resistor structure of claim 1 further comprising:
an inter layer dielectric positioned on the substrate, the inter layer dielectric
comprising at least a contact hole connecting to the salicide layer; and
25 at least a conductive layer positioned on portions of the surface of the inter layer

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dielectric and within the contact hole.

Claim 4 (original): The resistor structure of claim 1 further comprising an ion implantation well positioned underneath the semiconductor layer.

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Claim 5 (original): The resistor structure of claim 1 wherein the semiconductor layer comprises a polysilicon layer.

10 Claim 6 (original): The resistor structure of claim 5 further comprising a dielectric layer positioned underneath the semiconductor layer.

Claim 7 (original): A resistor structure comprising:
a substrate; and
a semiconductor layer positioned on the substrate, the semiconductor layer comprising at least a high resistance region and a low resistance region;
15 wherein the semiconductor layer comprises a predetermined region overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region, and the
20 semiconductor layer has a higher doping concentration within the predetermined region than in the other regions.

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Claim 8 (original): The resistor structure of claim 7 further comprising a salicide block positioned on the portions of the semiconductor layer within the high resistance region.

5 Claim 9 (original): The resistor structure of claim 8 further comprising a salicide layer positioned on the portions of the semiconductor layer within the low resistance region.

10 Claim 10 (original): The resistor structure of claim 9 wherein the predetermined region overlaps the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block.

15 Claim 11 (original): The resistor structure of claim 7 wherein the predetermined region is located at either end of the semiconductor layer.

20 Claim 12 (original): The resistor structure of claim 7 further comprising:
an inter layer dielectric positioned on the substrate, the inter layer dielectric comprising at least a contact hole connecting to the portions of the semiconductor layer within the low resistance region; and
at least a conductive layer positioned on portions of the surface of the inter layer dielectric and within the contact hole.

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Claim 13(original): The resistor structure of claim 7 further comprising an ion
implantation well positioned underneath the semiconductor layer.

5 Claim 14 (original): The resistor structure of claim 7 wherein the semiconductor layer
comprises a polysilicon layer.

Claim 15 (original): The resistor structure of claim 14 further comprising a dielectric
layer positioned underneath the semiconductor layer.

10 Claim 16-20 (cancelled)